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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,967	08/20/2003	Hiroyuki Nansei	030993	4992

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/643,967	NANSEI ET AL.	
	Examin r	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *12-38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-11* is/are rejected.

7)☒ Claim(s) *7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of the invention of Group I, claims 1-29, and Species I, claims 1-11, in the reply filed on 08 April 2004 is acknowledged. Claims 30-38 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Claims 12-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. *Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.*

The phrase "the memory cell" lacks antecedent basis (claim 5, line 5).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. *Claims 1, 3, 8, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Weimer (US 2003/0040171 A1).*

The Weimer US pre-grant published application (Weimer) discloses a method for manufacturing a semiconductor device (figs. 1-4 and accompanying text). The method comprises the following steps, **as recited in claim 1**: a step of forming a lower silicon oxide film 16 (fig. 1 and par. 23, lines 6-7); a step of forming a silicon film 18 on the lower silicon oxide film (fig. 2 and par. 24, lines 1-5); and a step of forming a silicon nitride film 20 on the lower silicon oxide film 16 to completely nitride the silicon film by a plasma nitriding method (fig. 3; par. 26, lines 1-10; and par. 28, lines 1-12), wherein a multilayered insulating film including at least the lower silicon oxide film and the silicon nitride film is formed (fig. 3).

The silicon film is formed under a temperature condition of 700°C or below, **as recited in claim 3** (par. 25, lines 1-8).

The silicon nitride film is formed by conducting nitriding processing in which plasma is excited by microwave in an atmosphere of a source gas containing nitrogen to generate a nitrogen radical, **as recited in claim 8** (par. 28, lines 1-12). The source gas containing nitrogen is selected from one of nitrogen (N_2) and ammonia (NH_3) (par. 28, lines 9-12). When nitrogen is used as the source gas, the source gas does not contain hydrogen, **as recited in claim 9**.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. *Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Weimer in view of Wolf (Silicon Processing for the VLSI Era – Vol. 2).*

Weimer lacks anticipation in not teaching that the silicon nitride film is a charge-storage film of a memory cell, **as recited in claim 4**.

Wolf discloses a method for forming an MNOS EEPROM device (page 628, §8.7.1). The MNOS EEPROM cell consists of a single MOS like transistor (page 628, §8.7.1, lines 1-3). The transistor's gate insulation film comprises a multilayered oxide-nitride (ON) film, wherein the nitride layer is a charge storage film (page 628, §8.7.1, lines 1-3).

Since Weimer and Wolf are from the same field of endeavor, the purpose disclosed in Wolf would have been recognized in the pertinent art of Weimer by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the ON multilayered film in an MNOS EEPROM cell, such that the silicon nitride film functions as a charge storage film, as taught by Wolf, since it is common to use an ON multilayered film as a gate insulation film in an MNOS EEPROM cell.

6. *Claims 1-3 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yashima (US 5,685,949) in view of Weimer.*

The Yashima patent (Yashima) discloses a method for manufacturing a semiconductor device (col. 9, line 41 - col. 11, line 6). The method comprises: a step of forming a lower silicon oxide film (col. 10, lines 1-18); a step of forming a silicon nitride film on the lower silicon oxide film by a plasma nitriding method (col. 10, lines 31-53), wherein a multilayered insulating film including at least the lower silicon oxide film and the silicon nitride film is formed.

An upper silicon oxide film is formed on the silicon nitride film by a plasma oxidizing method (col. 10, line 65 - col. 11, line 6), wherein the multilayered insulating film is composed of the lower silicon oxide film, the silicon nitride film, and the upper silicon oxide film, **as recited in claim 2.**

The silicon nitride film is formed by conducting nitriding processing in which plasma is excited by microwave in an atmosphere of a source gas containing nitrogen to generate a nitrogen radical, **as recited in claim 8** (col. 10, lines 44-53). The source gas does not contain hydrogen, **as recited in claim 9** (col. 10, lines 44-53).

The upper silicon oxide film is formed by conducting oxidizing processing in which plasma is excited by microwave in an atmosphere of a source gas containing oxygen to generate an oxygen radical, **as recited in claim 10** (col. 10, lines 1-18 and col. 10, line 65 – col. 11, line 6). The source gas does not contain hydrogen, **as recited in claim 11** (col. 10, lines 1-18).

Yashima does not teach forming a silicon film on the lower silicon oxide film; and completely nitriding the silicon film by a plasma nitriding process to form the silicon nitride film.

As stated above, Weimer discloses a method for manufacturing a semiconductor device. Again, the method comprises forming a silicon nitride film 20 on a silicon oxide film 16 (fig. 3), wherein a silicon film 18 is formed on the silicon oxide film (fig. 2 and par. 24, lines 1-5) and, using a plasma nitriding process, is subsequently completely nitrided to form the silicon nitride film (fig. 3; par. 26, lines 1-10; and par. 28, lines 1-12).

The silicon film is formed under a temperature condition of 700°C or below, **as recited in claim 3** (par. 25, lines 1-8).

The silicon nitride film is formed by conducting nitriding processing in which plasma is excited by microwave in an atmosphere of a source gas containing nitrogen to

generate a nitrogen radical, **as recited in claim 8** (par. 28, lines 1-12). The source gas containing nitrogen is selected from one of nitrogen (N_2) and ammonia (NH_3) (par. 28, lines 9-12). When nitrogen is used as the source gas, the source gas does not contain hydrogen, **as recited in claim 9**.

Since Yashima and Weimer are from the same field of endeavor, the purpose disclosed by Weimer would have been recognized in the pertinent reference of Yashima by one of ordinary skill in the art at the time the invention was made.

Weimer seeks to reduce the thickness of a silicon nitride film in a composite dielectric, such that the resulting overall effective oxide thickness obtained is desirable (par. 5, lines 7-14). Preferably the silicon film 18 has a thickness of 1 to 2 nm (par. 24, lines 11-13), which in turn results in the subsequently formed silicon nitride film having a thickness of 1 to 2 nm. The silicon nitride layer in Yashima is formed to a thickness of 2 nm (col. 10, lines 49-53). To reduce the thickness of the silicon nitride film from 2 nm to 1 nm, one of ordinary skill in the art would have been motivated to modify Yashima in view of Weimer at the time the invention was made.

7. *Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yashima in view of Weimer as applied to claim 2 above, and further in view of Su et al. (US 6,133,096).*

Yashima does not teach forming the multilayered oxide-nitride-oxide insulating film (ONO) as a dielectric film between a floating gate and a control gate in a memory cell, **as recited in claim 5**, or forming a gate insulation film in a peripheral circuit region

by the plasma oxidizing method simultaneously with the upper silicon oxide film, **as recited in claim 6.**

The Su et al. patent (Su) discloses a method for simultaneously forming a flash memory cell and peripheral devices (figs. 1-6, 7B, 8-15 and accompanying text). The method comprises: forming a multilayered ONO film 9 as a dielectric film between a floating gate 7b and a control gate 10, 11 in a memory cell region 70 (fig. 7B and col. 4, lines 42-46), wherein the multilayered ONO film is simultaneously formed as a gate insulation film 9 in a peripheral circuit region 80.

Since Yashima and Su are from the same field of endeavor, the purpose disclosed in Su would have been recognized in the pertinent art of Yashima by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Yashima and Weimer, by forming the multilayered ONO film as a dielectric between a floating gate and a control gate in a memory cell, as taught by Su, since an ONO composite dielectric is commonly used as an inter-poly dielectric in flash memory cells. Furthermore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Yashima and Weimer, by simultaneously forming the multilayered ONO film as a gate insulation film in a peripheral circuit region, as taught by Su, because a structure is formed that has dual gate insulation film thicknesses. High performance transistors, such as the stacked gate transistor require thinner gate

dielectric regions and operate at lower voltages, whereas most conventional external peripherals typically require higher operating voltages. When interfacing lower voltage high performance MOS transistors to higher voltage devices, input and output (I/O) buffers of the integrated circuit (IC) are typically designed to contain thicker gate dielectric regions that are compatible with the higher external peripheral device voltages.

Allowable Subject Matter

8. *Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.* There is no teaching or suggestion in the prior art of record to form the silicon film to a thickness of 5 nm or above. As discussed above, Weimer discloses a method of forming a silicon nitride film on a silicon oxide film, wherein a silicon film is formed on the silicon oxide film and is subsequently completely nitrided to form the silicon nitride film. The silicon film has a thickness of less than 30 Å, i.e. 3 nm (par. 24, lines 11-13). Thus, Weimer teaches away from forming the silicon film to a thickness of 5 nm or above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
10 June 2004

Mary Wilczewski
Primary Examiner